Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.236”**

**.240”**

**SOURCE**

**GATE**

**BACKSIDE IS DRAIN**

**Top Material: Al**

**Backside Material: Ti/Ni/Ag**

**Gate = .018 x .026 ”**

**Source = .051 X .069”**

**Backside Potential: Drain**

**APPROVED BY: DK DIE SIZE .236” X .240” DATE: 7/11/22**

**MFG: INT’L RECTIFIER THICKNESS .016” P/N: IRFC250BV**

**DG 10.1.2**

#### Rev B, 7/19/02